REMARKS

Claims 48-54 are pending in the present application.

Claim 51 stands rejected under 35 USC § 112, second paragraph. Pursuant to the suggestion of the Examiner, Claim 51 has been amended to depend from claim 49. Accordingly, the rejection of claim 51 under 35 USC § 112, second paragraph, is believed to be overcome.

Claims 48-50 and 50-54 stand rejected under 35 USC §102 (b) as being anticipated by United States Patent Number 5,346,838 to Ueno (Ueno).

The present invention relates to area efficient static memory cells employing parasitic bipolar transistors which can be latched in a bistable on state with small area transistors. Each bipolar transistor memory cell includes a gate which is pulse biased during a write operation to latch up the cell. Page 5, lines 7-13.

Claim 48 recites a method of forming a circuit for storing information as one of at least two possible stable current states, including providing a semiconductor substrate, and providing doped silicon regions to form a multi-region planar thyristor having at least four regions. At least one polysilicon gate is formed overlying a unique junction of the multi-region planar thyristor, thereby making the unique junction a gated diode, and connecting

the at least one polysilicon gate to a voltage source for producing latch-up in the multi-region planar thyristor.

Ueno describes an insulated gate control thyristor whose current capacity is on the order of several tens of Amperes including a plurality of unit structures which are repeated in a lateral direction. Column 7, lines 24-27. According to Ueno, each gate is patterned by growing polysilicon film, or the like, over the entire surface of the wafer, and then by carrying out reactive ion etching using CCl_4 and Cl_2 on the polysilicon film to form patterns covering substantially the entire surface of each chip. Subsequently, a plurality of narrow stripe-like windows are formed in a direction normal to the sheet of figure 3 as shown in Ueno. Alternate first and second windows are formed in such a manner that each of the windows is a few micrometers to 10 micrometers wide, and adjacent windows are each spaced approximately the same distance apart. Each gate patterned on the base region serves as a mask for a p-type impurity implantation followed by annealing to form an emitter layer and a collector layer. Column 7, lines 38-54. Subsequently, an n-type cathode layer is formed in the emitter layer under a first window to a depth of about one micron or less. Column 7, lines 62-64. The result, as is shown in figure 3, is a gate 20 overlying a plurality of junctions.

This is different from the structure claimed in claim 48, as amended, which claims forming at least one polysilicon gate overlying a unique junction of a multi-region planar thyristor, thereby making the unique junction a gated diode. The gate 20 of Ueno, as

shown in figure 3, overlies a plurality of junctions, and thereby serves to form a MOS transistor 71, as illustrated in the schematic diagram shown in figure 4 of Ueno. Accordingly, the gate structure of Ueno, which covers a plurality of junctions, is completely different from the gate structure of the presently claimed intervention which covers only a unique junction, and results in the formation of a gated diode 26 as shown, for example, in figure 2 of the present application. Accordingly, since the disclosure of Ueno does not teach or suggest the present invention as claimed, the rejection of claim 48 under 35 USC § 102 (b) is overcome.

Claims 49, 50 and 52-54 each depend directly or indirectly from claim 48, and incorporate every limitation thereof. Therefore, by the arguments presented above, the rejections of claims 40, 50 and 52-54 under 35 USC § 102 (b) are likewise overcome.

Claim 51 stands rejected under 35 USC § 103 (a) as being unpatentable over Ueno. As demonstrated by the foregoing arguments, however, the Ueno reference to entirely fails to teach the invention as claimed in claim 48, as amended. Since claim 51 depends indirectly from claim 48, the Ueno reference likewise fails to teach the invention as claimed in claim 51. Nor does the Ueno reference offer any suggestion that the art, as recited therein, be modified to include forming at least one polysilicon gate overlying a unique junction of a multi-region planar thyristor, thereby making the unique junction a gated diode.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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Version With Markings To Show Changes Made

48. (Amended) A method of forming a circuit for storing information as one of at least two possible stable current states, the method comprising the following steps:

providing a semiconductor substrate;

providing doped silicon regions to form a multi-region planar thyristor having at least four regions;

forming at least one polysilicon gate overlying a unique junction of said multi-region planar thyristor thereby making said unique junction a gated diode; and

connecting said at least one polysilicon gate to a voltage source for producing latch-up in said multi-region planar thyristor.

51. (Amended) The method of claim [50] 49 wherein said step of providing doped silicon regions further comprises forming an n-p-n-p-n-p-n planar thyristor.